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*DB=USPT; PLUR=YES; OP=ADJ*

<u>L9</u>	L8 and ((mode or standby or (data adj2 hold)) near8 (internal near3 clock))	25	<u>L9</u>
<u>L8</u>	L7 and l3 and l2	37	<u>L8</u>
<u>L7</u>	L6 and l5 and l4	213	<u>L7</u>
<u>L6</u>	data near8 (internal near3 clock)	2719	<u>L6</u>
<u>L5</u>	address near8 (internal near3 clock)	914	<u>L5</u>
<u>L4</u>	(command or request) near8 (internal near3 clock)	681	<u>L4</u>
<u>L3</u>	(clock near3 input\$3) near8 (external near2 clock) near8 (internal near3 clock)	437	<u>L3</u>
<u>L2</u>	SDRAM or (synchronous adj4 (memory or storage))	5889	<u>L2</u>
<u>L1</u>	5768213.pn.	1	<u>L1</u>

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l8 and l1	48

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<u>L7</u>	L6 and l5 and l4	207	<u>L7</u>
<u>L6</u>	(internal near3 clock) near8 data	2719	<u>L6</u>
<u>L5</u>	(internal near3 clock) near8 address	914	<u>L5</u>
<u>L4</u>	(internal near3 clock) near8 command	545	<u>L4</u>
<u>L3</u>	(internal near3 clock) near8 command	545	<u>L3</u>
<u>L2</u>	(internal near3 clock) near8 (hold or held or standby or (power adj down))	456	<u>L2</u>
<u>L1</u>	((365/\$)!.CCLS.)	32631	<u>L1</u>

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<u>L18</u>	L17 and (365/\$.ccls.)	59	<u>L18</u>
<u>L17</u>	L16 and (embedded or (one adj chip))	176	<u>L17</u>
<u>L16</u>	L15 and (memory adj2 control\$4)	620	<u>L16</u>
<u>L15</u>	L1 and LSI	3694	<u>L15</u>

*DB=PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ*

<u>L14</u>	L13 and ((clock adj2 (input or buffer)) near8 activ\$6)	1	<u>L14</u>
<u>L13</u>	L9 and ((input adj2 signal) near6 (compar\$3 or match\$4 or differ\$4 or correspond\$4) near8 (internal adj2 signal))	15	<u>L13</u>
<u>L12</u>	L9 and ((clock near3 (processor or system or external or internal)) near8 (command adj2 buffer) near8 ((hold or (power adj2 down)) adj2 (mode or state)))	2	<u>L12</u>
<u>L11</u>	L9 and ((clock near3 (buffer or input)) near8 (command adj2 input) near8 ((hold or (power adj2 down)) adj2 (mode or state)))	5	<u>L11</u>
<u>L10</u>	L9 and ((clock near3 (buffer or input)) near8 (clock adj2 line) near8 (normal adj2 (mode or state)))	1	<u>L10</u>
<u>L9</u>	(synchronous adj3 memory) or (semiconductor adj integrated adj circuit)	53537	<u>L9</u>

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L8</u>	l6 and ((clock adj2 (input or buffer)) near8 activ\$6)	1	<u>L8</u>
<u>L7</u>	l6 and ((clock adj2 buffer) near8 activ\$6)	0	<u>L7</u>
<u>L6</u>	L1 and ((input adj2 signal) near6 (compar\$3 or match\$4 or differ\$4 or correspond\$4) near8 (internal adj2 signal))	24	<u>L6</u>
<u>L5</u>	L1 and ((clock near3 (processor or system or external or internal)) near8 (command adj2 buffer) near8 ((hold or (power adj2 down)) adj2 (mode or state)))	0	<u>L5</u>
<u>L4</u>	L1 and ((clock near3 (processor or system or external or internal)) near8 (command adj2 input) near8 ((hold or (power adj2 down)) adj2 (mode or state)))	0	<u>L4</u>
<u>L3</u>	L1 and ((clock near3 (buffer or input)) near8 (command adj2 input) near8 ((hold or (power adj2 down)) adj2 (mode or state)))	1	<u>L3</u>
<u>L2</u>	L1 and ((clock near3 (buffer or input)) near8 (clock adj2 line) near8 (normal adj2 (mode or state)))	0	<u>L2</u>
<u>L1</u>	(synchronous adj3 memory) or (semiconductor adj integrated adj circuit)	22146	<u>L1</u>

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```
((synchronous <near/4> memory) or  
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((clock <near/2> (input or buffer))  
<sentence> (command <near/2> (input  
or buffer))) <sentence> ((hold or  
(power down) ) <near/2> (mode or  
state))
```

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